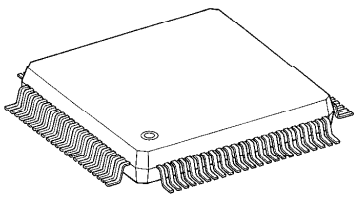
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# T6B08

## ROW DRIVER FOR A DOT MATRIX LCD

The T6B08 is a 68-channel-output row driver for an STN dot matrix LCD. The T6B08 features a −28-V LCD drive voltage. The T6B08 is able to drive LCD panels with a duty ratio of up to 1/240. It is recommended for use with the T6B07.



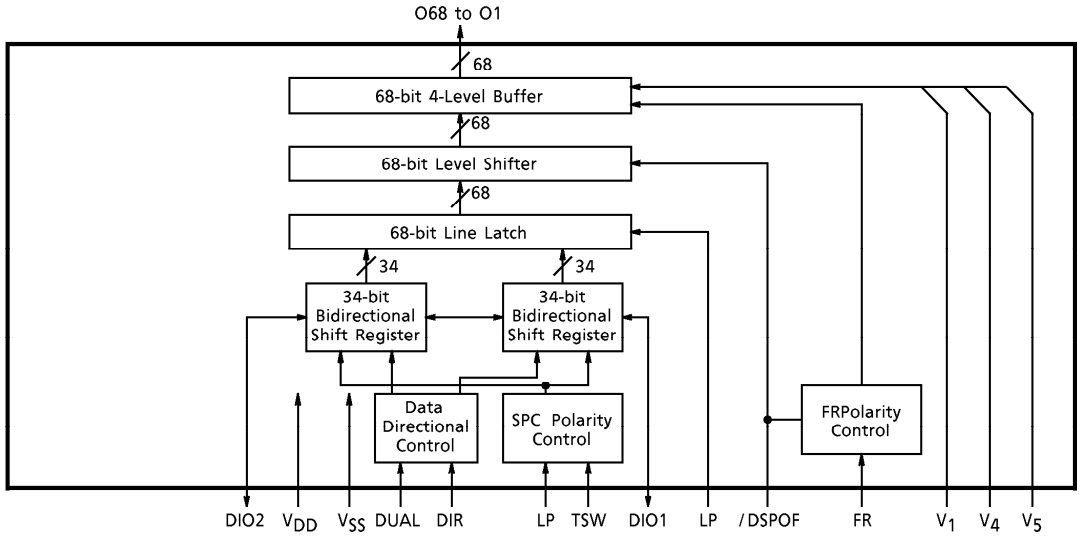
QFP92-P-1818-0.70B

Weight : 1.45g (typ.)

### FEATURES

- Display duty application : to 1/240
- LCD drive signal : 68
- Data transfer : 1-bit bidirectional
  ① O68←O1
  ② O68→O1
  ③ O1→O34, O68→O35
- LCD drive voltage : −11 to −28V (max −30V)
- Operating voltage : 3.0 to 5.5V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 1.2kΩ (max) (12.8V, 1/9 bias)
- Display-off function : When /DSPOF is L, all LCD drive outputs (O1 to O68) remain at the $V_{DD}$ level.
- LCD drive output timing : Change on falling edge of LP

### BLOCK DIAGRAM

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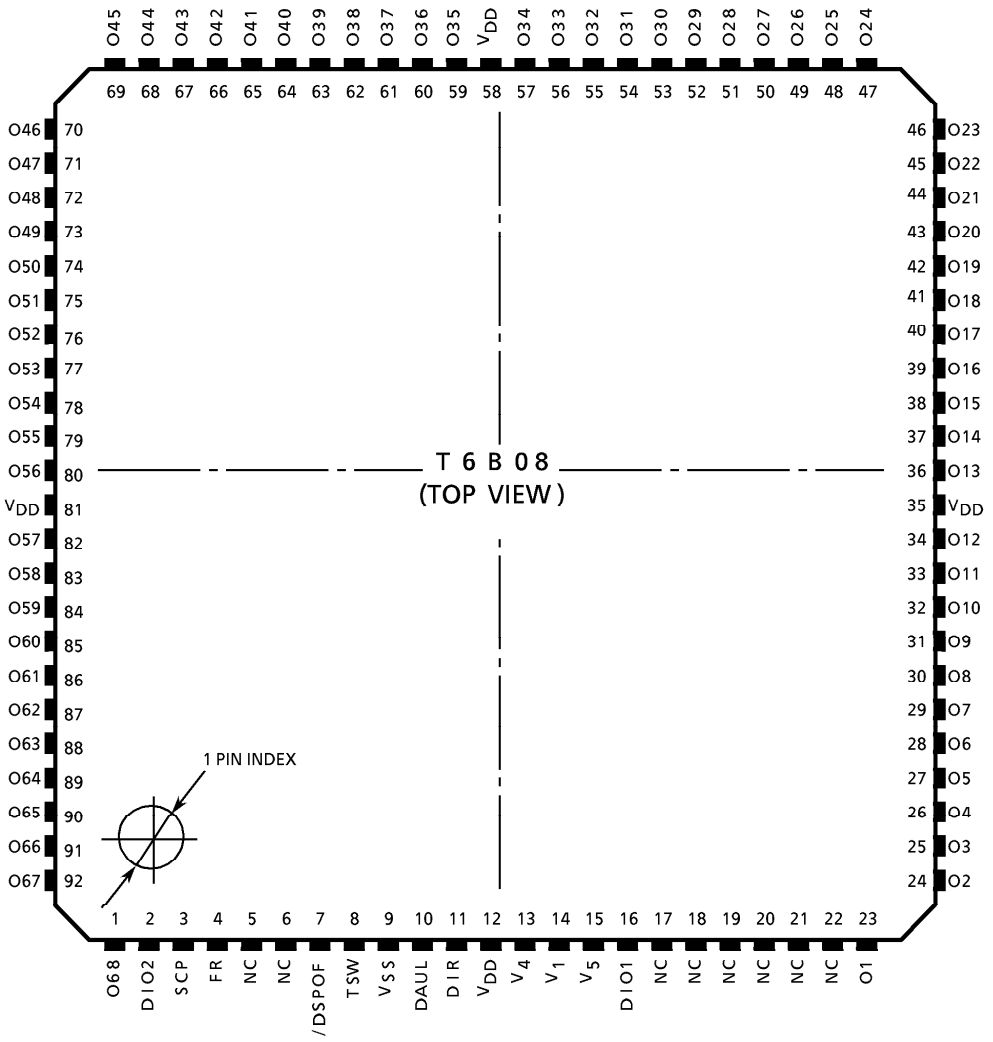
**PIN ASSIGNMENT**



**PIN FUNCTIONS**

| PIN NAME | I/O | FUNCTIONS | LEVEL |
|---|---|---|---|
| O1 to O68 | Output | Output for LCD drive signal | $V_{DD}$ to $V_5$ |
| DIO1, DIO2 | I/O | Input/output for shift data | $V_{DD}$ to $V_{SS}$ |
| LP | Input | (Shift Clock Pulse)<br>Input for shift clock pulse | |
| FR | Input | (Frame)<br>Input for frame signal | |
| DUAL | Input | (Dual Mode)<br>Terminal for dual input mode or single input mode select | |
| DIR | Input | (Direction)<br>Input for data flow direction select | |
| TSW | Input | (Terminal Switch)<br>When tied to $V_{SS}$: (O1 to O68) output on the rising edge of LP<br>When tied to $V_{DD}$: (O1 to O68) output on the falling edge of LP | |
| /DSPOF | Input | (Display Off)<br>/DSPOF = L: Display-off mode, (O1 to O68) remain at the $V_{DD}$ level.<br>/DSPOF = H: Display-on mode, (O1 to O68) are operational. | |
| $V_{DD}$ | — | Power supply for internal logic (5V) | — |
| $V_{SS}$ | — | Power supply for internal logic (0V) | |
| $V_1$ | — | Power supply for LCD drive circuit | |
| $V_4$ | — | Power supply for LCD drive circuit | |
| $V_5$ | — | Power supply for LCD drive circuit | |

RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

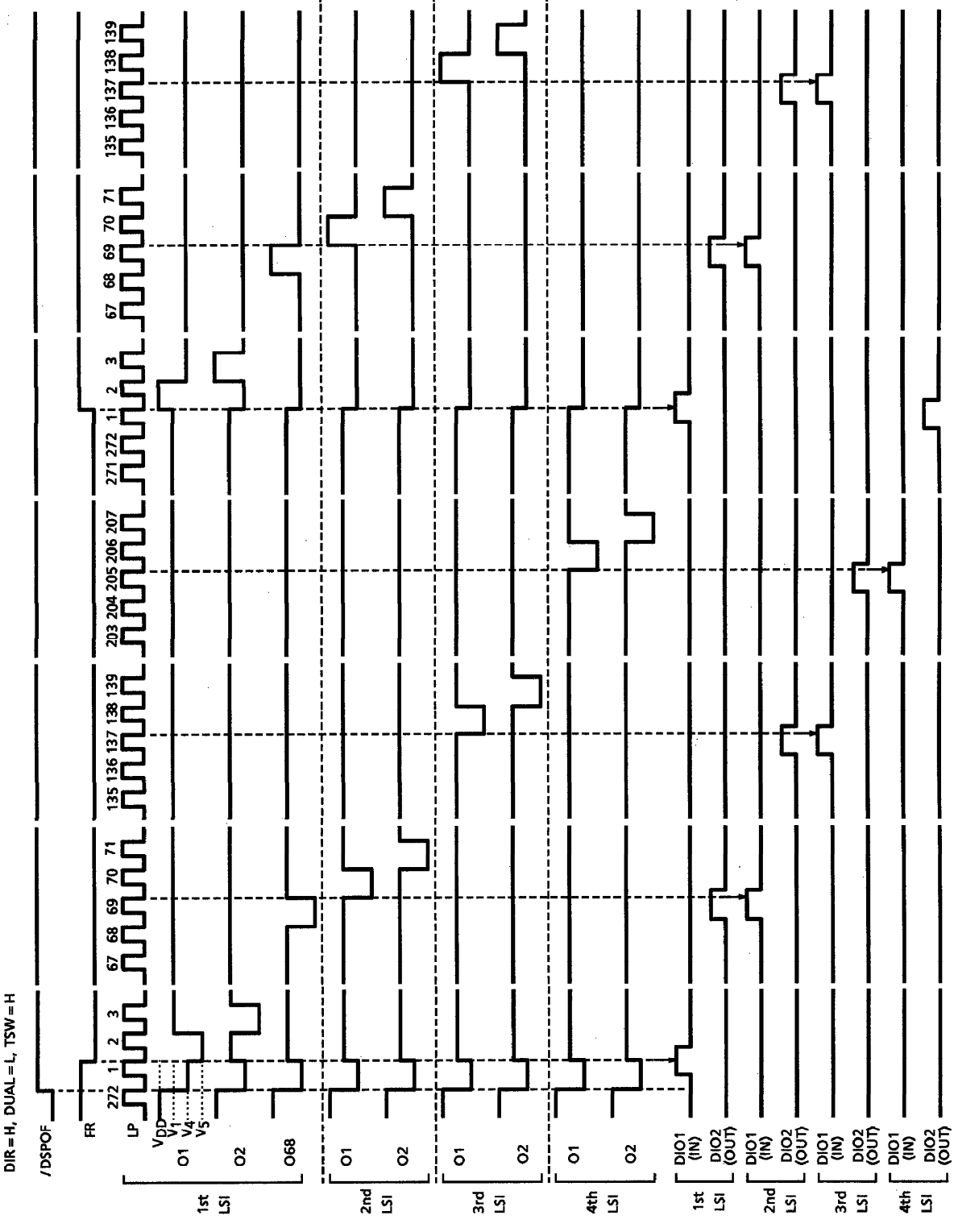
| F R | DATA INPUT (DIO1, DIO2) | /DSPOF | OUTPUT LEVEL |
|---|---|---|---|
| L | L | H | $V_1$ |
| L | H | H | $V_5$ |
| H | L | H | $V_4$ |
| H | H | H | $V_{DD}$ |
| * | * | L | $V_{DD}$ |

* Don't Care

DATA INPUT FORMAT

| DUAL | DIR | DATA FLOW | DATA INPUT | |
|---|---|---|---|---|
| | | | DIO1 | DIO2 |
| $V_{DD}$ | $V_{DD}$ | O1→O34 | IN | IN |
| | | O68→O35 | | |
| $V_{SS}$ | $V_{DD}$ | O1→O68 | IN | OUT |
| $V_{DD}$ | $V_{SS}$ | O68→O1 | OUT | IN |
| $V_{SS}$ | $V_{SS}$ | | | |

## TIMING DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

(Ensure that the following conditions are maintained, $V_{DD} \geqq V_1 \geqq V_4 \geqq V_5$, $V_{SS} = 0$)

| ITEM | SYMBOL | PIN NAME | RATING | UNIT |
|---|---|---|---|---|
| Supply Voltage 1 | $V_{DD}$ | $V_{DD}$ | −0.3 to 7.0 | V |
| Supply Voltage 2 | $V_1$<br>$V_4$<br>$V_5$ | $V_1$<br>$V_4$<br>$V_5$ | $V_{DD}$ − 30.0 to $V_{DD}$ + 0.3 | V |
| Input Voltage | $V_{IN}$ | (*1) | −0.3 to $V_{DD}$ + 0.3 | V |
| Operating Temperature | $T_{opr}$ | — | −20 to 75 | °C |
| Storage Temperature | $T_{stg}$ | — | −55 to 125 | °C |

(*1) LP, FR, /DSPOF, TSW, DUAL, DIR, DIO1, DIO2

**ELECTRICAL CHARACTERISTICS**

DC CHARACTERISTICS

TEST CONDITIONS (1) (Unless otherwise noted, $V_{SS} = 0V$, $V_{DD} = 4.5$ to $5.5V$, $V_5 = (V_{DD} - 28)$ to $(V_{DD} - 11)$ V, Ta = −20 to 75°C)

| ITEM | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|
| Supply Voltage 1 | | — | — | — | 4.5 | 5.0 | 5.5 | V | $V_{DD}$ |
| Supply Voltage 2 | | — | — | — | $V_{DD}$ − 28 | — | $V_{DD}$ − 11 | V | $V_5$ |
| Input Voltage | H Level | $V_{IH}$ | — | — | $V_{DD}$ − 0.8 | — | $V_{DD}$ | V | LP, FR, /DSPOF, TSW, DUAL, DIR, DIO1, DIO2 |
| | L Level | $V_{IL}$ | | — | 0 | — | 0.8 | | |
| Output Voltage | H Level | $V_{OH}$ | — | $I_{OH}$ = −0.5mA | $V_{DD}$ − 0.5 | — | $V_{DD}$ | V | DIO1, DIO2 |
| | L Level | $V_{OL}$ | | $I_{OL}$ = 0.5mA | 0 | — | 0.5 | | |
| Output Resistance | H Level | $R_{OH}$ | — | $V_{OUT} = V_{DD} - 0.5V$ (*2) | — | 0.65 | 1.2 | kΩ | O1 to O68 |
| | M Level | $R_{OM}$ | | $V_{OUT} = V_1 \pm 0.5V$ (*2) | — | 0.65 | 1.2 | | |
| | | $R_{OM}$ | | $V_{OUT} = V_4 \pm 0.5V$ (*2) | — | 0.65 | 1.2 | | |
| | L Level | $R_{OL}$ | | $V_{OUT} = V_5 + 0.5V$ (*2) | — | 0.65 | 1.2 | | |
| Current Consumption | | $I_{SS}$ | — | $V_{DD} = 5.5V$<br>$V_5 = -22.5V$<br>$f_{FR} = 35.5Hz$<br>$f_{LP} = 7.1kHz$<br>$f_{DIO} = 71Hz$<br>$V_{IH} = 5.5V$, $V_{IL} = 0V$ | — | 2.0 | 4.0 | μA | $V_{SS}$ |

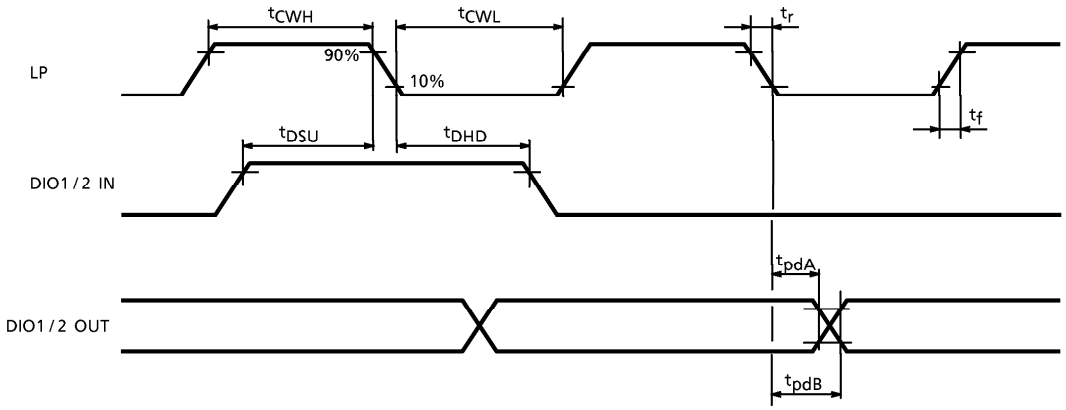
(*2) $V_{DD} = 5.0V$, $V_5 = -7.8V$, $V_1 = V_{DD}$-1 / 9 ($V_{DD}$-$V_5$), $V_4 = V_{DD}$-8 / 9 ($V_{DD}$-$V_5$)

TEST CONDITIONS (2) (Unless otherwise noted, $V_{SS}$ = 0V, $V_{DD}$ = 3.0 to 5.5V, $V_5$ = ($V_{DD}$ – 28) to ($V_{DD}$ – 11) V, Ta = – 20 to 75°C)

| ITEM | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|
| Supply Voltage 1 | | — | — | — | 3.0 | 3.3 | 5.5 | V | $V_{DD}$ |
| Supply Voltage 2 | | — | — | — | $V_{DD}$ – 28 | — | $V_{DD}$ – 11 | V | $V_5$ |
| Input Voltage | H Level | $V_{IH}$ | — | — | $V_{DD}$ – 0.6 | — | $V_{DD}$ | V | LP, FR, /DSPOF, TSW, DUAL, DIR, DIO1, DIO2 |
| | L Level | $V_{IL}$ | | — | 0 | — | 0.6 | | |
| Output Voltage | H Level | $V_{OH}$ | — | $I_{OH}$ = – 0.5mA | $V_{DD}$ – 0.5 | — | $V_{DD}$ | V | DIO1, DIO2 |
| | L Level | $V_{OL}$ | | $I_{OL}$ = 0.5mA | 0 | — | 0.5 | | |
| Output Resistance | H Level | $R_{OH}$ | — | $V_{OUT}$ = $V_{DD}$ – 0.5V (*3) | — | 0.65 | 1.2 | kΩ | O1 to O68 |
| | M Level | $R_{OM}$ | | $V_{OUT}$ = $V_1$ ± 0.5V (*3) | — | 0.65 | 1.2 | | |
| | | $R_{OM}$ | | $V_{OUT}$ = $V_4$ ± 0.5V (*3) | — | 0.65 | 1.2 | | |
| | L Level | $R_{OL}$ | | $V_{OUT}$ = $V_5$ + 0.5V (*3) | — | 0.65 | 1.2 | | |
| Current Consumption | | $I_{SS}$ | — | $V_{DD}$ = 5.5V<br>$V_5$ = – 22.5V<br>$f_{FR}$ = 35.5Hz<br>$f_{LP}$ = 7.1kHz<br>$f_{DIO}$ = 71Hz<br>$V_{IH}$ = 5.5V, $V_{IL}$ = 0V | — | 2.0 | 4.0 | μA | $V_{SS}$ |

(*3) $V_{DD}$ = 3.0V, $V_5$ = – 9.8V, $V_1$ = $V_{DD}$-1 / 9 ($V_{DD}$-$V_5$), $V_4$ = $V_{DD}$-8 / 9 ($V_{DD}$-$V_5$)

AC CHARACTERISTICS




TEST CONDITIONS (1) ($V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 5.5V, $V_5$ = ($V_{DD}$-28) to ($V_{DD}$-11) V, Ta = – 20 to 75°C)

| ITEM | SYMBOL | TEST CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SCP Pulse Width H | $t_{CWH}$ | LP | 40 | — | ns |
| SCP Pulse Width L | $t_{CWL}$ | LP | 1 | — | μs |
| Input Rise / Fall Time | $t_r$, $t_f$ | LP, FR, DIO1, DIO2 | — | (*6) | ns |
| Data Set-up Time | $t_{DSU}$ | DIO1, DIO2 | 40 | — | ns |
| Data Hold Time | $t_{DHD}$ | DIO1, DIO2 | 40 | — | ns |
| Output Data Delay Time A (*5) | tpdA | DIO1, DIO2 | 500 | — | ns |
| Output Data Delay Time B (*5) | tpdB | DIO1, DIO2 | — | 1 | μs |

TEST CONDITIONS (2) ($V_{SS}$ = 0V, $V_{DD}$ = 3.0 to 5.5V, $V_5$ = ($V_{DD}$-28) to ($V_{DD}$-11) V, Ta = – 20 to 75°C)

| ITEM | SYMBOL | TEST CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SCP Pulse Width H | $t_{CWH}$ | LP | 50 | — | ns |
| SCP Pulse Width L | $t_{CWL}$ | LP | 1 | — | μs |
| Input Rise / Fall Time | $t_r$, $t_f$ | LP, FR, DIO1, DIO2 | — | (*6) | ns |
| Data Set-up Time | $t_{DSU}$ | DIO1, DIO2 | 50 | — | ns |
| Data Hold Time | $t_{DHD}$ | DIO1, DIO2 | 50 | — | ns |
| Output Data Delay Time A (*5) | tpdA | DIO1, DIO2 | 700 | — | ns |
| Output Data Delay Time B (*5) | tpdB | DIO1, DIO2 | — | 1 | μs |

(*5) $C_L$ = 10pF

(*6) $t_r, t_f \leqq (t_C - t_{CWH} - t_{CWL}) / 2$ or $t_r, t_f \leqq 50$ns

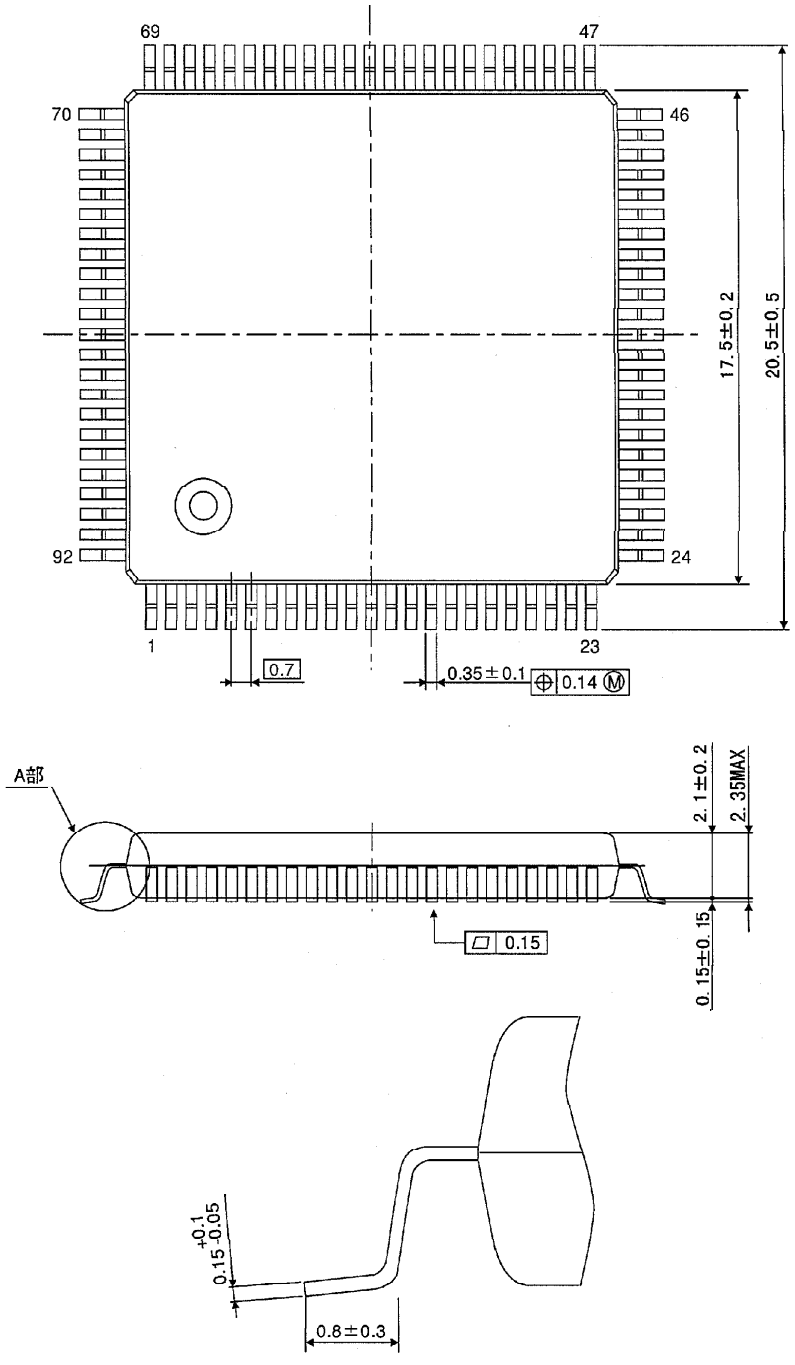
**NOTE**

Insert the bypass capacitor (0.1μF) between $V_{DD}$ and $V_{SS}$ to decrease the power supply noise. Place the bypass capacitor as close to the LSI as possible.

**OUTLINE DRAWING**

QFP92-P-1818-0.70B

Unit : mm




Weight : 1.45g (Typ.)